VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please replace the paragraph beginning at page 3, line 20 with the following paragraph:

The present invention concerns an apparatus comprising a circuit having one or more inputs. The [option] inputs may be configured to provide a device identification (ID) of one or more different device IDs. The one or more inputs may allow implementation of the circuit with one of the one or more different device IDs.

Please replace the paragraph beginning at page 17, line 1 with the following paragraph:

An apparatus comprising a circuit having one or more inputs. The one or more [option] inputs may be configured to provide a device identification (ID) of one or more different device IDs. The one or more inputs may allow implementation of the circuit with one of the one or more different device Ids.

IN THE CLAIMS

Please amend the claims as follows:

1. (AMENDED) An apparatus comprising:

a circuit comprising one or more inputs configured to provide a selected device identification (ID) from one of a plurality of different device IDs, wherein said one or more inputs allow said circuit to be implemented with said selected one of said plurality of different device IDs.

2. (AMENDED) The apparatus according to claim 1, wherein said selected device identification ID comprises a soft code.

3. (AMENDED) The apparatus according to claim 1, wherein said circuit comprises a JTAG compliant controller.

4. (AMENDED) The apparatus according to claim 1, wherein each of said plurality of different device IDs each provide a configuration of said circuit.

5. (AMENDED) The apparatus according to claim 1, wherein said selected device identification ID can be configured after fabrication of said apparatus.

6. (AMENDED) The apparatus according to claim 1, wherein said circuit comprises:

a logic circuit configured to receive said one or more inputs;

a multiplexer configured to receive an output of said logic circuit; and

a memory element configured to receive an output of said multiplexer.

7. The apparatus according to claim 6, wherein said multiplexer is further configured to receive an input signal and a shift signal.

8. The apparatus according to claim 7, wherein said logic circuit comprises a logic gate.

9. The apparatus according to claim 1, wherein said circuit is implemented within a FIFO memory.

10. The apparatus according to claim 1, wherein said one or more inputs comprise mark options.

11. The apparatus according to claim 1, wherein said one or more inputs comprise configuration input pins.

12. The apparatus according to claim 1, wherein said circuit comprises a JTAG device compliant with the IEEE standard 1149.1.

13. (AMENDED) An apparatus comprising:

means for receiving one or more inputs; and

means for providing a selected device identification (ID) from a plurality of different device IDs, wherein said one or more inputs allow implementation of said selected device ID.

14. (AMENDED) A method for selecting one of a multiple number device identifications (IDs) comprising the steps of:

(A) receiving one or more inputs; and

(B) selecting a device identification (ID) from a plurality of different device IDs, wherein said one or more inputs allow implementation of said selected device ID.

15. (AMENDED) The method according to claim 14, wherein said selected device identification ID comprises a soft code.

16. (AMENDED) The method according to claim 14, wherein each of said different device IDs each implement a circuit configuration.

17. (AMENDED) The method according to claim 14, wherein said selected device identification ID can be configured after fabrication.

18. The method according to claim 14, wherein said one or more inputs comprise mark options.

19. The method according to claim 14, wherein said one or more inputs comprise configuration input pins.

20. The method according to claim 14, further comprising providing a JTAG device compliant with the IEEE standard 1149.1.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a circuit comprising one or more inputs configured to provide a selected device identification (ID) [of] from one [or more] of a plurality of different device IDs, wherein said one or more inputs allow said circuit to be implemented with said selected one of said [one or more] plurality of different device IDs.

2. (AMENDED) The apparatus according to claim 1, wherein said selected device identification ID comprises a soft code.

3. (AMENDED) The apparatus according to claim 1, wherein said circuit comprises a JTAG compliant controller.

4. (AMENDED) The apparatus according to claim 1, wherein each of said [one or more] plurality of different device IDs [comprise] each provide a configuration of said circuit.

5. (AMENDED) The apparatus according to claim 1, wherein said selected device identification ID can be configured after fabrication of said apparatus.

6. (AMENDED) The apparatus according to claim 1, wherein said circuit comprises:

a logic circuit configured to receive said one or more inputs;

a [multiplier] multiplexer configured to receive an output of said logic circuit; and

a memory element configured to receive an output of said multiplexer.

13. (AMENDED) An apparatus comprising:

means for receiving one or more inputs; and

means for providing a selected device identification (ID) [of one or more] from a plurality of different device IDs, wherein said one or more inputs allow implementation of said [one or more different] selected device [IDs] ID.

14. (AMENDED) A method for selecting one of a multiple number device identifications (IDs) comprising the steps of:

(A) receiving one or more inputs; and

(B) [providing] selecting a device identification (ID) [of one or more] from a plurality of different device IDs, wherein said one or more inputs allow implementation of said [one or more different] selected device [IDs] ID.

15. (AMENDED) The method according to claim 14, wherein said selected device identification ID comprises a soft code.

16. (AMENDED) The method according to claim 14, wherein each of said [one or more] different device IDs [comprise] each implement a circuit configuration.

17. (AMENDED) The method according to claim 14, wherein said selected device identification ID can be configured after fabrication.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a circuit having one or more inputs. The one or more inputs may be configured to provide selected a device identification (ID) from a plurality of different device IDs. The one or more inputs may allow the circuit to be implemented with the selected one of the plurality of different device IDs.

CLAIM OBJECTIONS

The objection to claim 6 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-4, 6-16, and 18-20 under 35 U.S.C. §102(b) as being anticipated by the background of the present application and is traversed, in part, and obviated, in part, and should be withdrawn.

The presently claimed invention is not disclosed by the background section of the present application. However, independent claims 1, 13 and 14 have been amended to clarify the present invention. The background section of the present application does not disclose multiple configurations of a device

ID (e.g., see page 3, lines 14-17 of the background). In particular, the background section of the present application does not disclose or suggest selecting a device identification from one of a plurality of different device IDs, as presently claimed. As such, the presently claimed invention is fully patentable over the background section and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 5 and 17 under 35 U.S.C. §103(a) as being obvious over Swoboda '824 (or Carmichael '311) is respectfully traversed and should be withdrawn.

While Swoboda may teach selecting an operational mode (see column 5, line 1) and Carmichael may disclose configuring and/or testing a FPGA (column 4, lines 7 and 8), neither Swoboda nor Carmichael discloses or suggests configuring a selected device identification ID after fabrication of the apparatus, as presently claimed. The mere statement that it would have been obvious to combine the background of the present application with Swoboda (or Carmichael) to enable convenient test and/or device reconfiguration which would enable better testing facilities (see paragraph 17 of the Office Action) merely provides hindsight reconstruction in the present invention based on Applicant's disclosure. There is no motivation in either Swoboda or Carmichael to provide such a

combination. As such, claims 5 and 17 are independently patentable over the cited references and the rejection should be withdrawn.

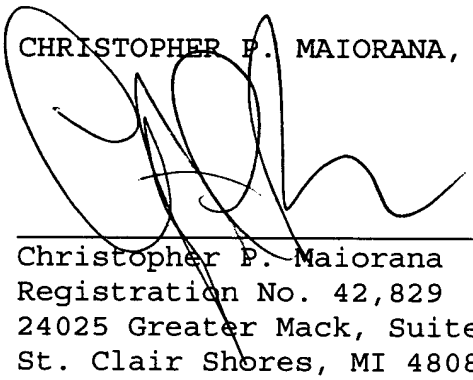
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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